**Hardware Development Plan**

1. Scope:  
   The following plan lays out the how the team will approach the Verilog Stopwatch project. The first section will cover the standards that apply to this project. The Second section covers how life cycle data will be tracked throughout the development cycle. The third and final section covers the different software and tools that will be used throughout the project.
2. Purpose:  
   The primary purpose of the project is for all team members to become sufficient with system Verilog. Secondary purposes include learning the Jira software, and gaining further exposure to and experience with DO-254.
3. Standards:

The following documents will define the standards for which this project will uphold with regards to coding practices, requirements generation, and branching strategies.

* 1. [Coding Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7BD717F7B6-E49C-4A3D-8979-9C33B494EDD0%7D&file=Coding%20Standards.docx&action=default&mobileredirect=true&CT=1591630910639&OR=ItemsView).v1
  2. [Requirements Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B9B8D3923-8CBC-4A8B-835B-5399245B6A96%7D&file=Requirements%20Standards.docx&action=default&mobileredirect=true&CT=1591630925910&OR=ItemsView).v1
  3. [Branching Strategy Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B2C639C94-C1F3-44DD-9050-C09DAD3E4F11%7D&file=Branching%20strategy.docx&action=default&mobileredirect=true&CT=1591630951111&OR=ItemsView).v1

1. Hardware Life-Cycle Data:

The following is how we will track the progress of our project. As the project evolves we will record life-cycle data to analyze and draw conclusions from upon completion of the project.

* 1. Life-Cycle Tracking Metrics:
     1. Number of git commits and new or edited lines of code shall be recorded at the end of stages 2, 3, and 4.
     2. Jira *Burndown Charts* and *Cumulative Flow Diagrams* shall be saved at the end of each sprint.
  2. Project Stages:
     1. Stage 0: Training & Planning, Deadline: 06/09
     2. Stage 1: Requirements Generation, Deadline: 06/11
        1. Generate Requirements
        2. Generate traceable testcases
        3. Requirements and Testcase Review/Sign-off
     3. Stage 2: Coding and Implementation, Deadline: 06/14
        1. Develop individual modules
        2. Write generic testbench for the module
        3. Review/Sign-off on source code and generic testbench
     4. Stage 3: Functional Verification, Deadline: 06/18
        1. Develop self reporting testbench
        2. Review/Sign-off on final testbench and module
     5. Stage 4: FPGA Integration, Deadline: 06/19

1. Developments Environment:

Below is a list of the tools the team will use as well as how or when the will be utilized during the project.

* 1. Requirements & Tools: Requirements are written in Excel according to the standards above and then signed off on using a checklist in Word.
  2. Design & Tools: Design and functionality specifications are written in word.
  3. Coding & Tools: Xilinx Vivado shall be used for developing, compiling, and testing our source code.
  4. Compiler/Linker: xsim shall be used when simulating source code.
  5. Hardware: Digilent Nexys A7 shall be used for FPGA integration.